**Name:**

**CSCE A342**

**Worksheet #3**

**Due 4/5/18**

**Problem 1 (50 points)**

**Assume:**

* **a register clock-to-Q propagation delay of 0.4 ns**
* **a register setup time of 0.3ns**
* **propagation delay of combinational logic 1 of 6 ns**
* **propagation delay of combinational logic 2 of 4 ns**
* **propagation delay of combinational logic 3 of 3 ns**

**What is the minimum latency of the following circuit?**

**What is the maximum throughput of the following circuit?**

Combinational Logic 1

Combinational Logic 2

Combinational

Logic 3

CLK

CLK

**What is the minimum latency of the following circuit (note the additional register)?**

**What is the maximum throughput of the following circuit?**

Combinational Logic 1

Combinational Logic 2

Combinational

Logic 3

CLK

CLK

CLK

**Problem 2 (50 points)**

**Create a circuit that counts the number of times a button on the BASYS 3 has been pressed. The counter should be displayed on the 7 segment led. The input button should be debounced and synchronized.**

**In addition to uploading the project source files, demonstrate the counter in class or upload a video of your FPGA to Blackboard to verify functionality.**